Remarks

The above-referenced application has been reviewed in light of the Examiner's Office Action dated January 24, 2007. Claims 1-20 are currently pending in this application. The Examiner's reconsideration of the rejections is respectfully requested, particularly in view of the above amendments and the following remarks.

As a preliminary matter, the Examiner's inaccurate and/or incomplete citation to Applicant's Admitted Prior Art has led to a significant delay in the filing of this response. Said prior art was cited by the Examiner only as "applicant's prior art" directly after a discussion of Applicant's prior patent, and referenced "paragraph 21", where the 21st sequential paragraph of the Application as filed, which shows line numbers rather than paragraph numbers, fell squarely within the Summary of the Invention section rather than within the Background section.

No other citation information was revealed until the undersigned contacted the Examiner at Applicant's request on April 10, 2007. At that time, the Examiner kindly indicated that he had intended to cite to the published version of the present application, namely U.S. Patent Application Publication No. 2004-0109517. Such citation was omitted from the Office Action mailed on January 24, 2007. Therefore, Applicant respectfully requests that the 76 day delay caused by the Examiner's error be included in the Patent Term Adjustment of any resulting patent in accordance with 35 U.S.C. § 154(b).

In accordance with the Office Action, Figures 1-4 of the drawings drew objections for failing to recite a legend such as "Prior Art". Said figures were rendered, interpreted and/or commissioned by Applicant, and not copied from the prior art. Applicant neither believes nor admits that said Figures show prior art for all purposes. *See, e.g.,* 35 U.S.C. § 103(c). The drawings have been amended to recite the legend "Background" to make clear that such subject matter is not intended to be claimed in the present application.

In accordance with the Office Action, Claims 1-8 stand rejected under the judicially created doctrine of non-statutory double patenting. Unfortunately, this judicially created doctrine does not currently address the logistics of typical patent prosecution in correspondence with the legal doctrines of notice or informed consent, particularly since all claims to be issued are typically subject to the disclaimer rather than merely the rejected claims. A proper Terminal Disclaimer disclaiming all extension to the patent term for all claims to be allowed and issued may be prepared once the Applicant can be advised as to which claims will be allowed.

In the present case, all of the currently pending claims are further rejected under 35 U.S.C. § 103(a). Accordingly, a Terminal Disclaimer, or the alternative cancellation of all claims rejected under the doctrine, may be timely filed upon the Examiner's indication of allowable subject matter.

In accordance with the Office Action, read in light of the telephone clarification of April 10, 2007, Claims 1-20 stand rejected under 35 U.S.C. §

103(a) as being unpatentable over U.S. Patent No. 5,918,040 to Jarvis in view of Applicant's Admitted Prior Art ("AAPA"). This rejection is traversed.

Claim 1 recites, *inter alia,* "A digital system comprising: a master circuit, which includes a circuit to detect clock delay . . . and a slave circuit . . . wherein the circuit to detect clock delay generates the reset control signal in response to the system reset signal or an internal reset signal, detects a delay between the output clock signal and the input clock signal, and loads and unloads the input data in response to an initial parameter corresponding to the delay."

The '040 to Jarvis is generally directed towards a method of synchronizing the timers of two processors. The method of Jarvis detects and synchronizes the timers of two networked processors by increasing the lesser of two timer values to match the greater value. The '040 falls short with respect to various elements of each of Applicant's presently pending claims. For example, the method of Jarvis uses one of two required circuits to synchronize its timers depending on which of the two timers is ahead. In addition, the method of Jarvis' fails to "input data that is synchronized with the input clock signal" and detect "a delay between the output clock signal and the input clock signal", both as recited in Claim 1.

At page 11 of the Office Action, last paragraph, the Examiner makes a rejection of Claim 1 while deferring to the later rejection of Claim 12 for the requisite motivation to combine. Beginning at page 14, last paragraph, the Examiner makes the rejection of Claim 12 while resting the motivation to

combine on Applicant's Background section. Continuing at page 15 of the Office Action, 2nd paragraph, the Examiner mis-interprets and/or mis-characterizes Applicant's Background section by stating, "These initial parameters are computed once synchronization is achieved". It is actually Applicant's Claim 1 that recites, *inter alia,* "wherein the circuit to detect clock delay . . . detects a delay between the output clock signal and the input clock signal, and loads and unloads the input data in response to an initial parameter corresponding to the delay". AAPA neither teaches nor fairly suggests that these "initial parameters are computed once synchronization is achieved", much less setting an initial parameter corresponding to the delay between an output clock signal and an input clock signal as effectively claimed by Applicant. Similarly, each of Claims 3 and 12 recite comparable features.

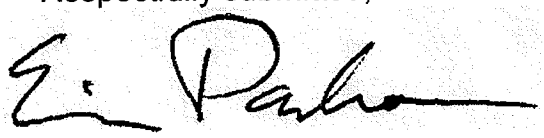
As mentioned above with respect to the drawings, Applicant has introduced certain material in the Background section in order to facilitate a more expedient introduction in the Detailed Description of the features that Applicant intends to claim as the invention. That is, while Applicant may consider features introduced in the Background section to be mere background with respect to the salient features discussed in the Detailed Description section, such introduction does not amount to an admission that either the Background section as a whole or the drawings discussed therein show "prior art" for all purposes. *See, e.g.,* 35 U.S.C. § 103(c). The currently claimed features are neither known nor admitted to be "prior art".

Accordingly, Claims 1, 3 and 12 are neither taught nor suggested by U.S. Patent No. 5,918,040 to Jarvis in view of AAPA, whether taken alone or in combination with any of the other properly available references of record in this case. If the Examiner intends to cite to references mentioned in Applicants' Background section and/or included in an Information Disclosure Statement, it is respectfully requested that the Examiner cite directly to such references, such as by U.S. Patent Number, for example.

Conclusion:

Accordingly, it is respectfully submitted that independent Claims 1, 3 and 12 are in condition for allowance for at least the reasons stated above. Since the remaining dependent claims each depend from one of the above claims and necessarily include each of the elements and limitations thereof, it is respectfully submitted that these claims are also in condition for allowance for at least the reasons stated, as well as for reciting additional patentable subject matter. Thus, each of Claims 1-20 is in condition for allowance. All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case are earnestly solicited.

Respectfully submitted,

By: 

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